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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, CUONG QUANG	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,875	KRUEGER ET AL.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *9-11,18,19,and 24- 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12-17,20-23 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02-07-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of species of Fi.5B, claims 1-8, 10,12-24, 27-31 is acknowledged. It is noted that, if all of above claims allowed, the claims depend on above claims also would be allowed.

It is noted that the limitations in claims 10 (the chip has side surface that comprise at least one step), 18 and 19 (a contact metallization on side surfaces of the chip that face the carrier substrate), 24 (the support element corresponds to a boundary of an indentation on the carrier substrate) are not in elected species Fig.5B. So, these claims also have been withdrawn from consideration.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 6, 8, 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The expression "the composite forming a seal with the carrier substrate outside of an area that corresponds to the chip" in claims 5, 6 is unclear. It is unclear what the term "with" means in this expression.

The expression "wherein the shrink frame forms a seal with the carrier substrate" in claim 8 is unclear. It is unclear what the term "with" means in this expression.

The expression "the dielectric forming a seal with the carrier substrate only in areas that do not correspond to the support....." in claim 13 is unclear. It is unclear what the term "with" means in this expression.

The expression "that forms a seal with the carrier substrate outside of an area that corresponds to the support element" in claim 17 is unclear. It is unclear what the term "with" means in this expression.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 14, 16, 20-22, 28, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Bureau et al. (US 6,492,194).

Regarding claims 1, 2, Bureau et al. discloses a component comprising: a chip having a top surface and having a bottom surface that includes electrically conductive tructures; a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip chip arrangement on the carrier substrate via electrically conductive connections (bumps) between the electrically conductive structures and the

connecting areas; a support element (107) at the top surface of the carrier substrate, the support element surrounding the chip but not touching the chip; and a seal that borders the chip and the support element, wherein the support element supports the seal. See Fig.4a.

Regarding claims 3, 4, 20, 21, 22, as shown in Bureau et al.'s Fig.4a, wherein the seal comprises a plastic layer (40) and substantially covers the top surface of the chip.

Regarding claim 7, as shown in Bureau et al.'s Fig.4a, the support element comprises a shink frame that substantially encloses the chip.

Regarding claim 14, as shown in Bureau et al.'s Fig.5, the dielectric layer (80) completely covering the top surface of the chip and sealing the support element, wherein the support element comprising a hermitically tight material.

Regarding claim 16, as shown in Bureau et al.'s Fig.4a, a layer (70) is considered as a filling compound on the dielectric layer (40).

Regarding claim 28, as shown in Bureau et al.'s Fig.4a, the carrier substrate including surface-mounted-device-capable contacts on its bottom surface.

Regarding claim 31, as shown in Bureau et al.'s Fig.4a, the device further comprising similar chips that are attacked the carrier substrate and that are similarly encapsulated.

Claims 1-2, 7, and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Bivona et al. (US 5,990,418).

Regarding claims 1, 2, Bivona et al. discloses a component comprising: a chip having a top surface and having a bottom surface that includes electrically conductive tructures; a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip chip arrangement on the carrier substrate via electrically conductive connections (bumps) between the electrically conductive structures and the connecting areas; a support element (a hermitically tight material 110) at the top surface of the carrier substrate, the support element surrounding the chip but not touching the chip; and a seal (104) that borders the chip and the support element, wherein the support element supports the seal. See Bivona's Fig.1-2.

Regarding claim 7, as shown in Bivona et al.'s Fig.1, the support element comprises a shink frame that substantially encloses the chip.

Regarding claim 27, Bivona et al. teaches that the carrier substrate is formed of ceramic. See claim 11.

Regarding claim 28, as shown in Bivona et al.'s Fig.2, the carrier substrate including surface-mounted-device-capable contacts on its bottom surface.

Claims 1-2 and 28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Ando et al. (US 6,433,412).

Regarding claims 1, 2, Bivona et al. discloses a component comprising: a chip having a top surface and having a bottom surface that includes electrically conductive tructures; a carrier substrate having a top surface that includes connecting areas, the chip being mounted in a flip chip arrangement on the carrier substrate via electrically

conductive connections (bumps) between the electrically conductive structures and the connecting areas; a support element (12) at the top surface of the carrier substrate, the support element surrounding the chip but not touching the chip; and a seal (11) that borders the chip and the support element, wherein the support element supports the seal. See Ando et al.'s Fig.1-2.

Regarding claim 28, as shown in Ando et al.'s Fig.2, the carrier substrate including surface-mounted-device-capable contacts on its bottom surface.

Regarding claim 29, as shown in Ando et al.'s Fig.2, the carrier substrate comprising at least two dielectric layers (each of metalizations layer being formed on a dielectric layer).

The limitation "low temrature cofired" in claim 27 is taken to be a product by process limitation, it is the patentability of the claimed product and not of recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the

patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12, 15, 23, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bureau et al.

Regarding claims 12 and 15, Bureau et al. teaches that the layer (60) is a conductive layer above the seal (40) relative to the top surface of the chip, the layer (60) being on edge areas of the support element. However, Bureau et al. but does not explicitly teach that the conductive layer is a metal layer.

It is conventional that metal is commonly used to form a conductive layer in a semiconductor device because metal has excellence electrical and thermal conductivities.

So, it would have been obvious to one of ordinary skill in the art to form the conductive layer (60) in Bureau et al.'s device by a metal layer in order to obtain a conductive layer with excellence electrical and thermal conductivity properties.

Regarding claim 23, the rejection of claim 23 is based on the same reasons as applied in claims 12 and 15 above.

Regarding claim 30, Bureau et al. teach that the chip is related to a surface acoustic wave filter (col.1 lines 1-25). However, Bureau et al. does not explicitluy teach that at least one resonator works with the acoustic surface waves.

it would have been obvious to one of ordinary skill in the art to form the chip that including a resonator as claimed because it is conventional and known in the art that resonator is commonly formed in the chip in order to work with the acoustic surface waves.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong Nguyen whose telephone number is (571) 272-1661. The examiner can normally be reached on 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cuong Nguyen

Primary examiner

2/19/07